LV8729V PWM Constant-Current Control Stepping Motor Driver

Overview

The LV8729V is a PWM current-controlled microstep bipolar stepping motor driver.
This driver can perform eight times of excitation of the second phase to 32W1-second phase and can drive simply by the CLK input.

Features

- Single-channel PWM current control stepping motor driver.
- BiCDMOS process IC.
- Output on-resistance (upper side : 0.35Ω ; lower side : 0.3Ω ; total of upper and lower : 0.65Ω ; Ta = 25°C, IO = 1.8A)
- 2-phase, 1-2 phase, W1-2 phase, 2W1-2 phase, 4W1-2 phase, 8W1-2 phase, 16W1-2 phase, 32W1-2 phase excitation are selectable.
- Advance the excitation step with the only step signal input.
- Available forward reverse control.
- Over current protection circuit.
- Thermal shutdown circuit. • Input pull down resistance • With reset pin and enable pin.

Specifications

Absolute Maximum Ratings at Ta = 25°C

Parameter	Symbol	Conditions	Ratings	Unit
Maximum supply voltage	VM max		36	V
Maximum output peak current	IO max		1.8	A
Maximum logic input voltage	VIN max		6	V
Maximum VREF input voltage	VREF max		6	V
Maximum MO input voltage	VMO max		6	V

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Parameter	Symbol	Conditions	Ratings	Unit
Maximum DOWN input voltage	VDOWN max		6	V
Allowable power dissipation	Pd max	*	3.85	W
Operating temperature	Topr		-30 to +85	°C

Storage temperature	Tstg		-55 to +150	°C

* Specified circuit board : 90.0mm×90.0mm×1.6mm, glass epoxy 2-layer board, with backside mounting.

Allowable Operating Ratings at Ta = 25°C

Parameter	Symbol	Conditions	Ratings	Unit
Supply voltage range	VM		9 to 32	V
Logic input voltage	VIN		0 to 5	V
VREF input voltage range	VREF		0 to 3	V

Electrical Characteristics at Ta = 25°C, VM = 24V, VREF = 1.5V

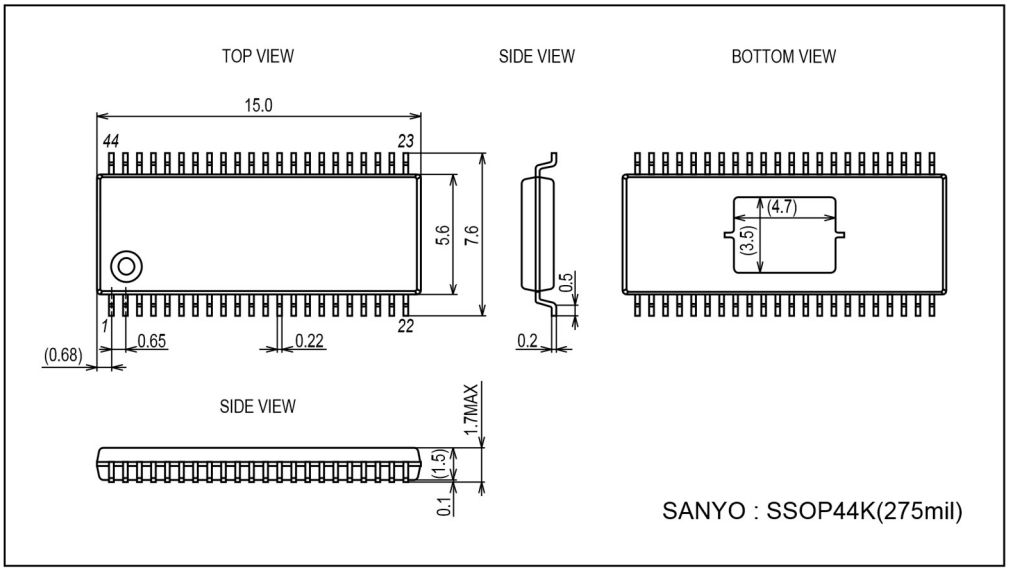
Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Standby mode current drain	IMst	ST = “L”		70	100	μA
Current drain	IM	ST = “H”, OE = “H”, no load		3.3	4.6	mA
Thermal shutdown temperature	TSD	Design guarantee	150	180	200	°C
Thermal hysteresis width	ΔTSD	Design guarantee		40		°C
Logic pin input current	IINL	V_{IN} = 0.8V	3	8	15	μA
	IINH	VIN = 5V	30	50	70	μA
Logic high-level input voltage	VINH		2.0			V
Logic low-level input voltage	VINL				0.8	V
Chopping frequency	Fch	Cosc1 = 100pF	70	100	130	kHz
OSC1 pin charge/discharge current	Iosc1		7	10	13	μA
Chopping oscillation circuit threshold voltage	Vtup1		0.8	1	1.2	V
	Vtdown1		0.3	0.5	0.7	V
VREF pin input voltage	Iref	VREF = 1.5V	-0.5			μA
DOWN output residual voltagr	V_{O}1DOWN	Idown = 1mA		40	100	mV
MO pin residual voltage	V_{O}1MO	Imo = 1mA		40	100	mV
Hold current switching frequency	Fdown	Cosc2 = 1500pF	1.12	1.6	2.08	Hz
Hold current switching frequency threshold voltage	Vtup2		0.8	1	1.2	V
	Vtdown2		0.3	0.5	0.7	V
VREG1 output voltage	Vreg1		4.7	5	5.3	V
VREG2 output voltage	Vreg2	VM	18	19	20	V
Output on-resistance	Ronu	I_O = 1.8A, high-side ON resistance		0.35	0.455	Ω
	Rond	I_O = 1.8A, low-side ON resistance		0.3	0.39	Ω
Output leakage current	IOleak	V_M = 36V			50	μA

Diode forward voltage	VD	ID = -1.8A		1	1.4	V
Current setting reference voltage	VRF	VREF = 1.5V, Current ratio 100%	0.285	0.3	0.315	V

Package Dimensions

unit : mm (typ)

3333



Pin Assignment

OUT1A

OUT1A

PGND1

NC

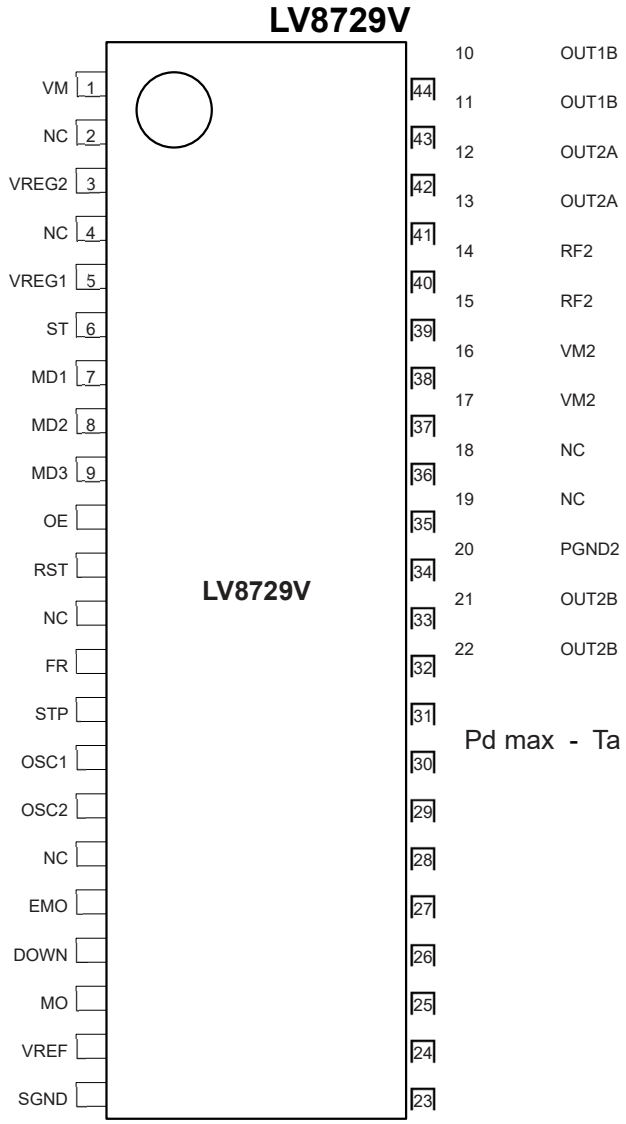
NC

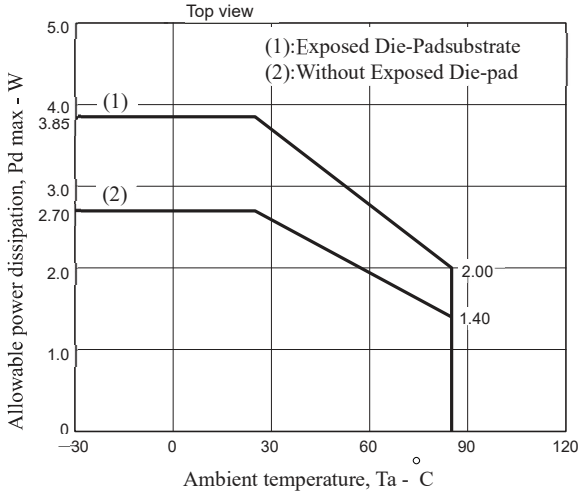
VM1

VM1

RF1

RF1



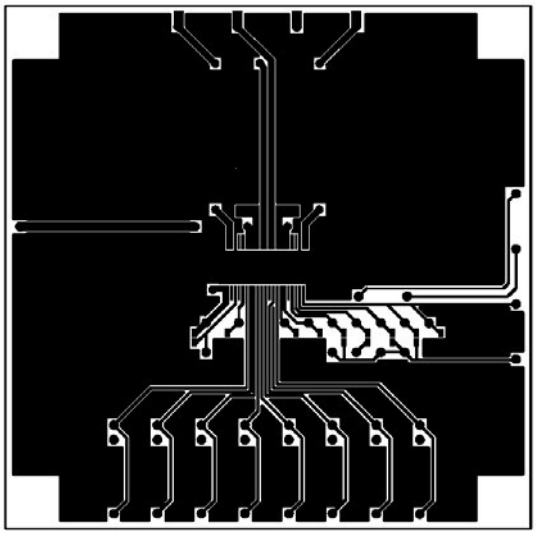


Substrate Specifications (Substrate recommended for operation of LV8729V)

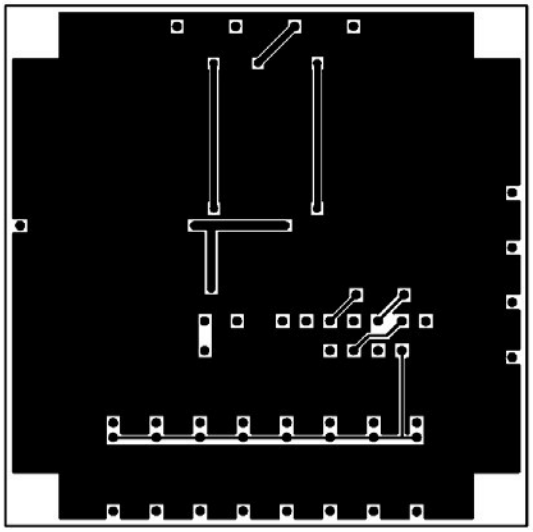
Size : 90mm × 90mm × 1.6mm (two-layer substrate [2S0P])

Material : Glass epoxy

Copper wiring density : L1 = 85% / L2 = 90%



L1 : Copper wiring pattern diagram



L2 : Copper wiring pattern diagram

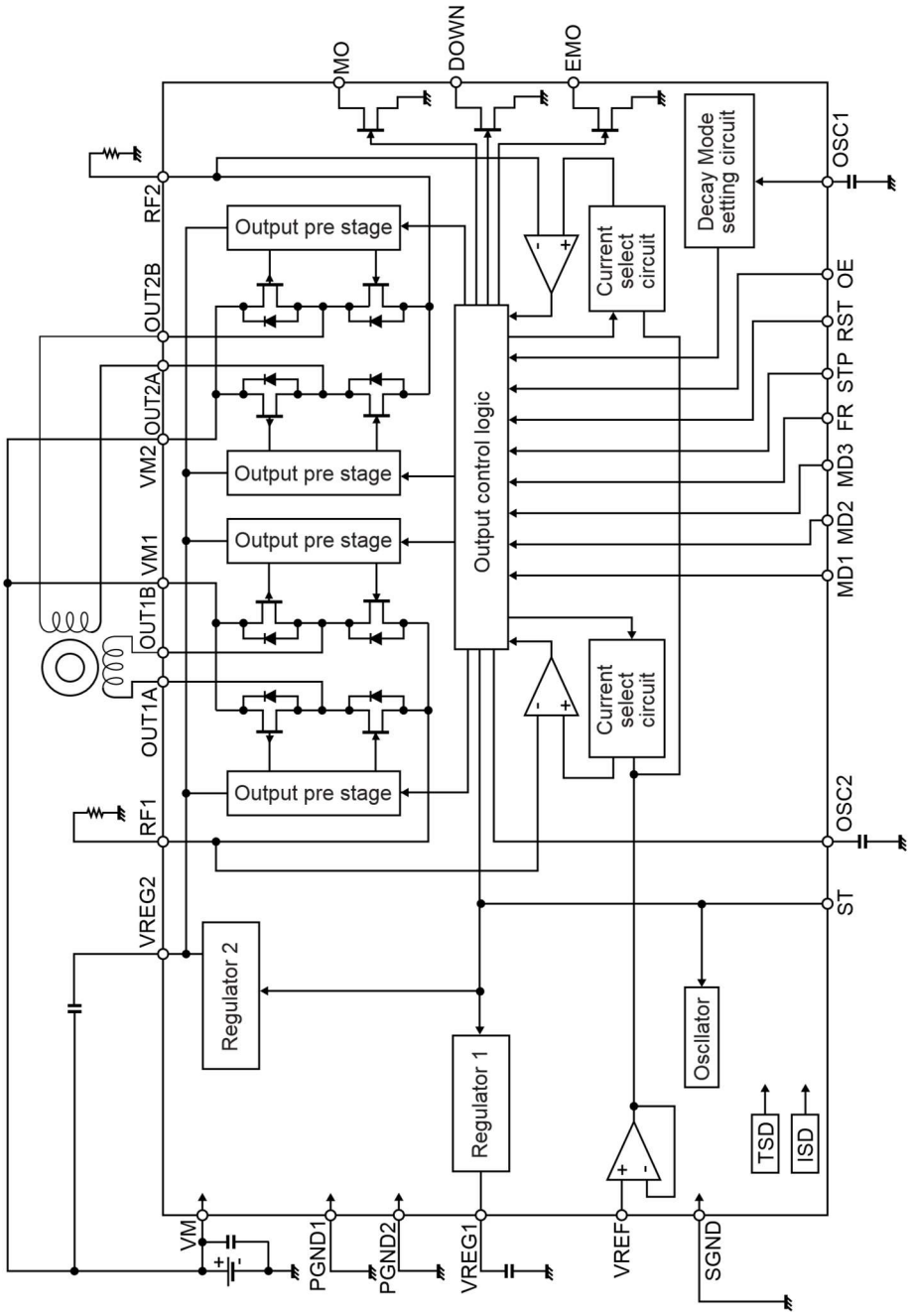
Cautions

1) The data for the case with the Exposed Die-Pad substrate mounted shows the values when 90% or more of the Exposed Die-Pad is wet.

2) For the set design, employ the derating design with sufficient margin.
Stresses to be derated include the voltage, current, junction temperature, power loss, and mechanical stresses such as vibration, impact, and tension.
Accordingly, the design must ensure these stresses to be as low or small as possible.
The guideline for ordinary derating is shown below :
(1)Maximum value 80% or less for the voltage rating
(2)Maximum value 80% or less for the current rating
(3)Maximum value 80% or less for the temperature rating

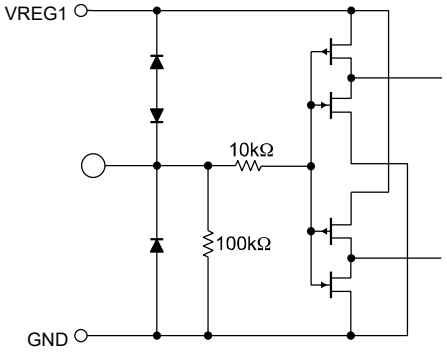
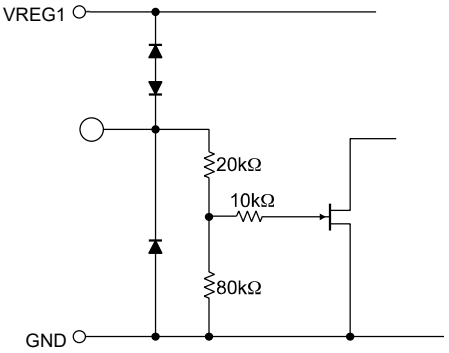
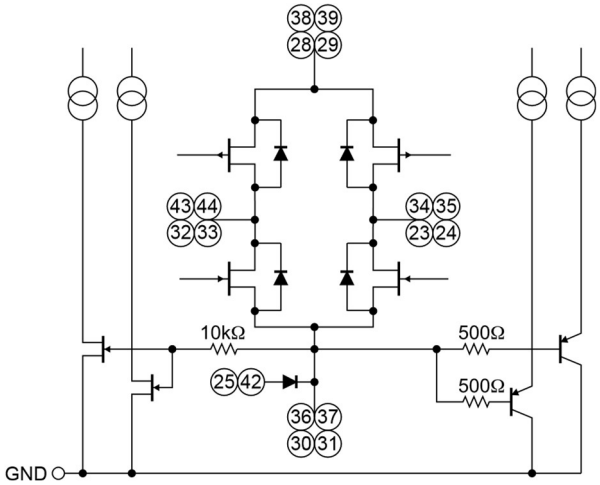
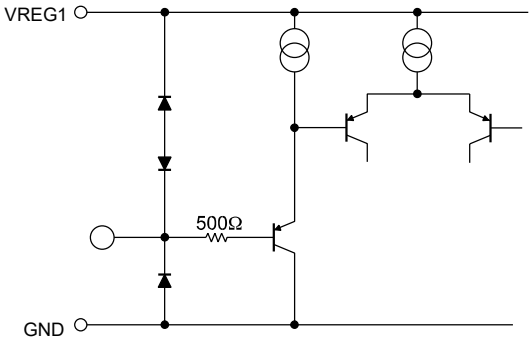
3) After the set design, be sure to verify the design with the actual product.
Confirm the solder joint state and verify also the reliability of solder joint for the Exposed Die-Pad, etc.
Any void or deterioration, if observed in the solder joint of these parts, causes deteriorated thermal conduction, possibly resulting in thermal destruction of IC.

Block Diagram



Pin Functions

Pin No.	Pin Name	Pin Functtion	Equivalent Circuit

7 8 9 10 11 13 14	MD1 MD2 MD3 OE RST FR STP	Excitation mode switching pin Excitation mode switching pin Excitation mode switching pin Output enable signal input pin Reset signal input pin Forward / Reverse signal input pin Step clock pulse signal input pin	
6	ST	Chip enable pin.	
23, 24 25 28, 29 30, 31 32, 33 34, 35 36, 37 38, 39 42 43, 44	OUT2B PGND2 VM2 RF2 OUT2A OUT1B RF1 VM1 PGND1 OUT1A	Channel 2 OUTB output pin. Channel 2 Power system ground Channel 2 motor power supply connection pin. Channel 2 current-sense resistor connection pin. Channel 2 OUTA output pin. Channel 1 OUTB output pin. Channel 1 current-sense resistor connection pin. Channel 1 motor power supply pin. Channel 1 Power system ground Channel 1 OUTA output pin.	
21	VREF	Constant-current control reference voltage input pin.	

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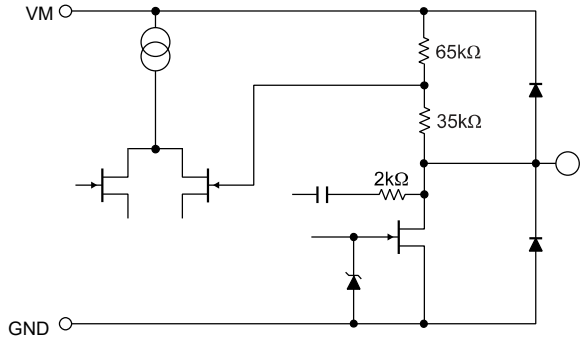
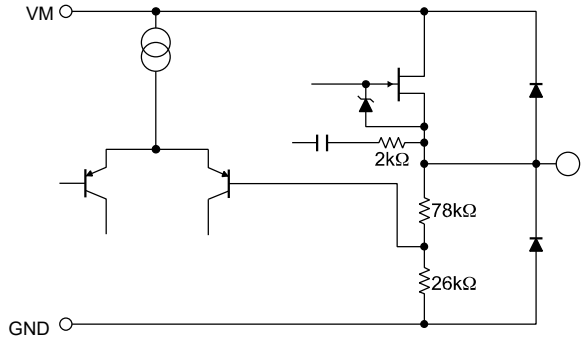
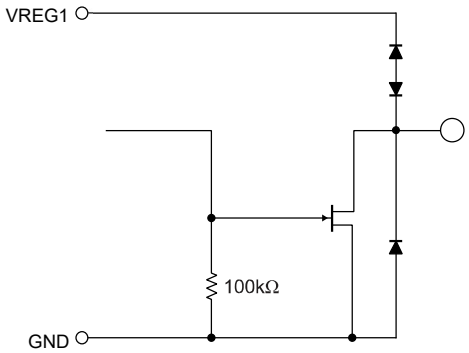
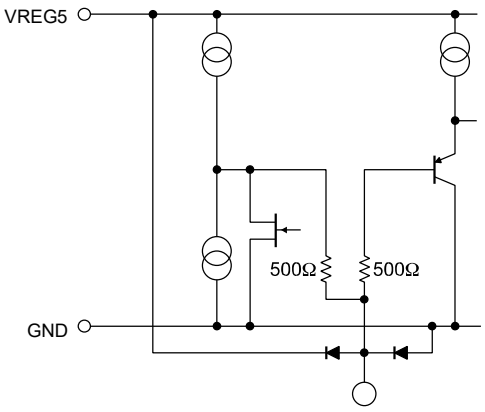
Pin No.	Pin Name	Pin Functtion	Equivalent Circuit

3	VREG2	Internal regulator capacitor connection pin.	
5	VREG1	Internal regulator capacitor connection pin.	
18 19 20	EMO DOWN MO	Over-current detection alarm output pin. Holding current output pin. Position detecting monitor pin.	
15 16	OSC1 OSC2	Copping frequency setting capacitor connection pin. Holding current detection time setting capacitor connection pin.	

Reference describing operation

(1) Stand-by function

When ST pin is at low levels, the IC enters stand-by mode, all logic is reset and output is turned OFF. When ST pin is at high levels, the stand-by mode is released.

(2) STEP pin function

Input	Operating mode

ST	STP	
Low	*	Standby mode
High	↑	Excitation step proceeds
High	↓	Excitation step is kept

(3) Excitation setting method

Set the excitation setting as shown in the following table by setting MD1 pin, MD2 pin and MD3 pin.

Input			Mode (Excitation)	Initial position	
MD3	MD2	MD1		1ch current	2ch current
Low	Low	Low	2 phase	100%	-100%
Low	Low	High	1-2 phase	100%	0%
Low	High	Low	W1-2 phase	100%	0%
Low	High	High	2W1-2 phase	100%	0%
High	Low	Low	4W1-2 phase	100%	0%
High	Low	High	8W1-2 phase	100%	0%
High	High	Low	16W1-2 phase	100%	0%
High	High	High	32W1-2 phase	100%	0%

The initial position is also the default state at start-up and excitation position at counter-reset in each excitation mode.

(4) Output current setting

Output current is set shown below by the VREF pin (applied voltage) and a resistance value between RF1(2) pin and GND.

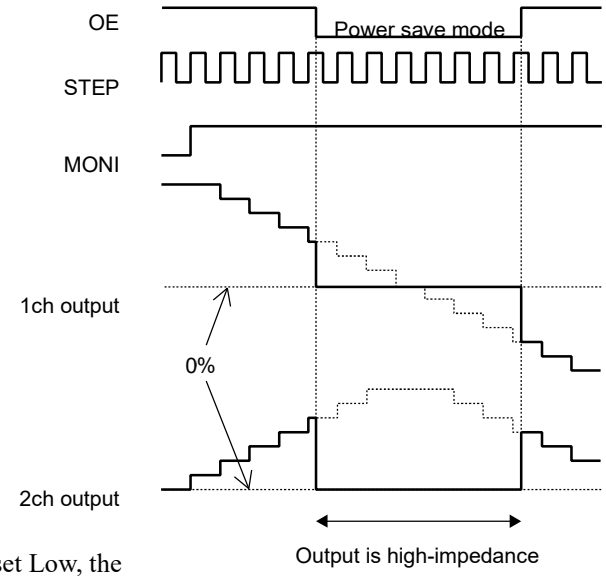
IOUT = (VREF / 5) / RF1 (2) resistance

* The setting value above is a 100% output current in each excitation mode.

(Example) When VREF = 1.1V and RF1 (2) resistance is 0.22Ω, the setting is shown below. IOUT = (1.1V / 5) / 0.22Ω = 1.0A

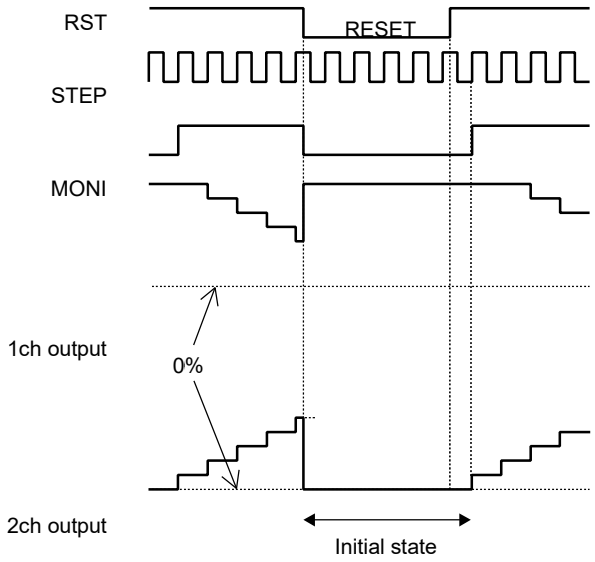
(5) Output enable function

When the OE pin is set Low, the output is forced OFF and goes to high impedance. However, the internal logic circuits are operating, so the excitation position proceeds when the STP is input. Therefore, when OE pin is returned to High, the output level conforms to the excitation position proceeded by the STP input.



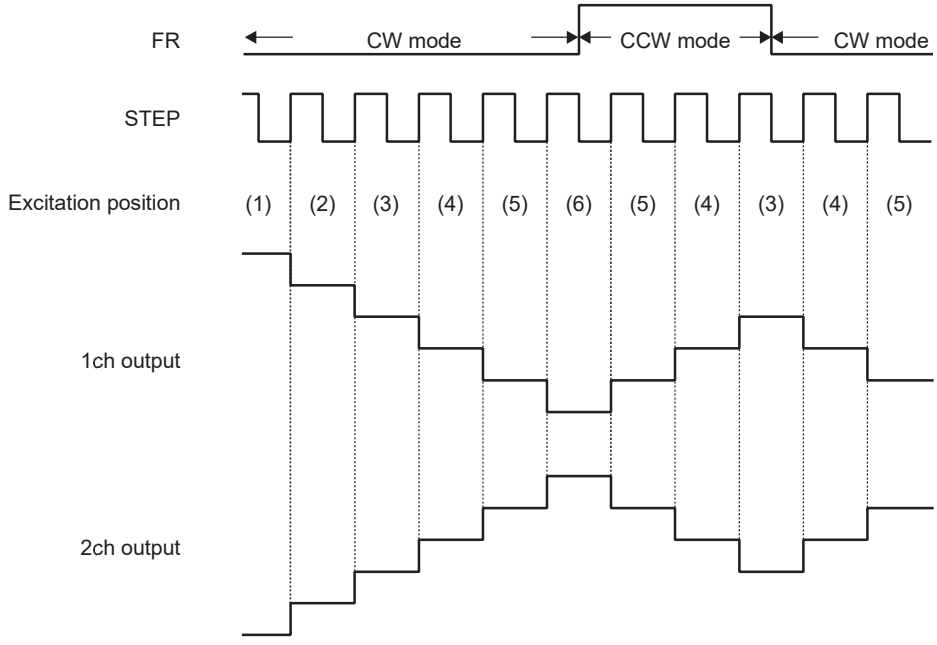
(6) Reset function

When the RST pin is set Low, the output goes to initial mode and excitation position is fixed in the initial position for STP pin and FR pin input. MO pin outputs at low levels at the initial position. (Open drain connection)



(7) Forward / reverse switching function

FR	Operating mode
Low	Clockwise (CW)
High	Counter-clockwise (CCW)



The internal D/A converter proceeds by a bit on the rising edge of the step signal input to the STP pin. In addition, CW and CCW mode are switched by FR pin setting.
In CW mode, the channel 2 current phase is delayed by 90° relative to the channel 1 current.
In CCW mode, the channel 2 current phase is advanced by 90° relative to the channel 1 current.

(8) EMO, DOWN, MO output pin

The output pin is open -drain connection. When it becomes prescribed, it turns on, and each pin outputs the Low level.

Pin state	EMO	DOWN	MO

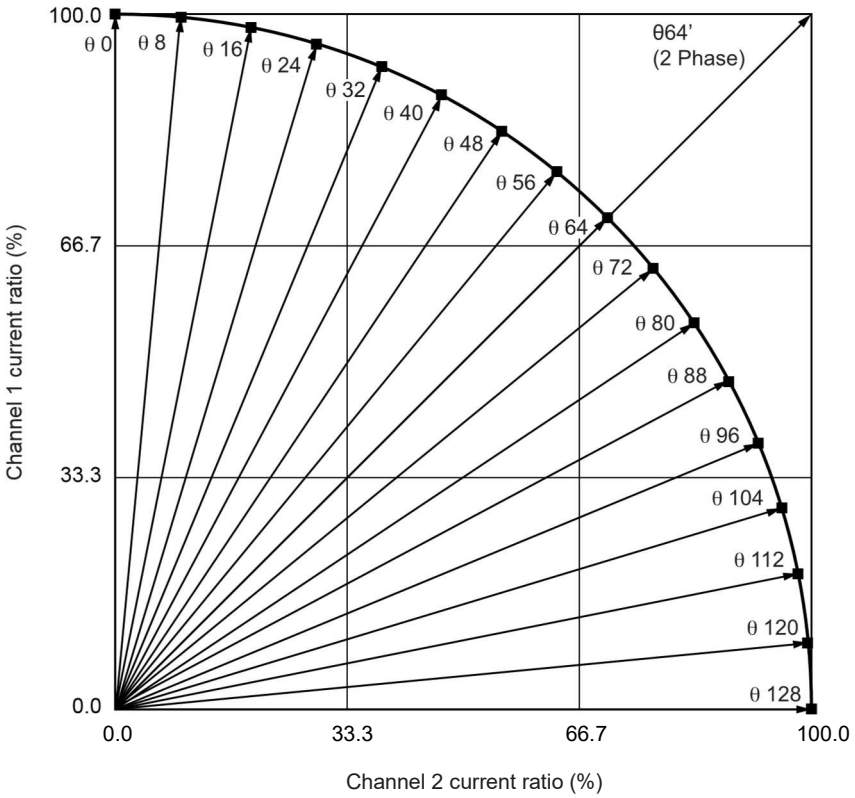
Low	At detection of over-current	Holding current state	Initial position
OFF	Normal state	Normal state	Non initial position

(9) Chopping frequency setting function

Chopping frequency is set as shown below by a capacitor between OSC1 pin and GND. Fcp = 1 / (Cosc1 / 10 x 10^{-6}) (Hz)

(Example) When Cosc1 = 200pF, the chopping frequency is shown below. Fcp = 1 / (200 x 10^{-12} / 10 x 10^{-6}) = 50(kHz)

(10) Output current vector locus (one step is normalized to 90 degrees)



Current setting ratio in each excitation mode

STEP	32W1-2 phase(%)		16W1-2 phase(%)		8W1-2 phase(%)		4W1-2 phase(%)		2W1-2 phase (%)		W1-2 phase (%)		1-2 phase (%)		2 phase (%)	
	1ch	2ch	1ch	2ch	1ch	2ch	1ch	2ch	1ch	2ch	1ch	2ch	1ch	2ch	1ch	2ch
θ0	100	0	100	0	100	0	100	0	100	0	100	0	100	0		
θ1	100	1														
θ2	100	2	100	2												
θ3	100	4														
θ4	100	5	100	5	100	5										
θ5	100	6														
θ6	100	7	100	7												
θ7	100	9														

θ8	100	10	100	10	100	10	100	10								
θ9	99	11														
θ10	99	12	99	12												
θ11	99	13														
θ12	99	15	99	15	99	15										
θ13	99	16														
θ14	99	17	99	17												
θ15	98	18														
θ16	98	20	98	20	98	20	98	20	98	20						
θ17	98	21														
θ18	98	22	98	22												
θ19	97	23														
θ20	97	24	97	24	97	24										
θ21	97	25														
θ22	96	27	96	27												
θ23	96	28														
θ24	96	29	96	29	96	29	96	29								
θ25	95	30														

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STEP	32W1-2 phase		16W1-2 phase		8W1-2 phase		4W1-2 phase		2W1-2 phase		W1-2 phase (%)		1-2 phase (%)		2 phase (%)	
	1ch	2ch	1ch	2ch	1ch	2ch	1ch	2ch	1ch	2ch	1ch	2ch	1ch	2ch	1ch	2ch
θ26	95	31	95	31												
θ27	95	33														
θ28	94	34	94	34	94	34										
θ29	94	35														
θ30	93	36	93	36												
θ31	93	37														
θ32	92	38	92	38	92	38	92	38	92	38	92	38				
θ33	92	39														
θ34	91	41	91	41												

θ35	91	42														
θ36	90	43	90	43	90	43										
θ37	90	44														
θ38	89	45	89	45												
θ39	89	46														
θ40	88	47	88	47	88	47	88	47								
θ41	88	48														
θ42	87	49	87	49												
θ43	86	50														
θ44	86	51	86	51	86	51										
θ45	85	52														
θ46	84	53	84	53												
θ47	84	55														
θ48	83	56	83	56	83	56	83	56	83	56						
θ49	82	57														
θ50	82	58	82	58												
θ51	81	59														
θ52	80	60	80	60	80	60										
θ53	80	61														
θ54	79	62	79	62												
θ55	78	62														
θ56	77	63	77	63	77	63	77	63								
θ57	77	64														
θ58	76	65	76	65												
θ59	75	66														
θ60	74	67	74	67	74	67										
θ61	73	68														
θ62	72	69	72	69												
θ63	72	70														
θ64	71	71	71	71	71	71	71	71	71	71	71	71	71	71	100	100

θ65	70	72														
θ66	69	72	69	72												
θ67	68	73														
θ68	67	74	67	74	67	74										
θ69	66	75														
θ70	65	76	65	76												
θ71	64	77														
θ72	63	77	63	77	63	77	63	77								
θ73	62	78														
θ74	62	79	62	79												
θ75	61	80														
θ76	60	80	60	80	60	80										
θ77	59	81														
θ78	58	82	58	82												
θ79	57	82														
θ80	56	83	56	83	56	83	56	83	56	83						
θ81	55	84														
θ82	53	84	53	84												
θ83	52	85														
θ84	51	86	51	86	51	86										
θ85	50	86														
θ86	49	87	49	87												
θ87	48	88														
θ88	47	88	47	88	47	88	47	88								
θ89	46	89														
θ90	45	89	45	89												

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STEP	32W1-2 phase		16W1-2 phase		8W1-2 phase		4W1-2 phase		2W1-2 phase		W1-2 phase (%)		1-2 phase (%)		2 phase (%)	
	1ch	2ch	1ch	2ch	1ch	2ch	1ch	2ch	1ch	2ch	1ch	2ch	1ch	2ch	1ch	2ch
θ91	44	90														

θ92	43	90	43	90	43	90										
θ93	42	91														
θ94	41	91	41	91												
θ95	39	92														
θ96	38	92	38	92	38	92	38	92	38	92	38	92				
θ97	37	93														
θ98	36	93	36	93												
θ99	35	94														
θ100	34	94	34	94	34	94										
θ101	33	95														
θ102	31	95	31	95												
θ103	30	95														
θ104	29	96	29	96	29	96	29	96								
θ105	28	96														
θ106	27	96	27	96												
θ107	25	97														
θ108	24	97	24	97	24	97										
θ109	23	97														
θ110	22	98	22	98												
θ111	21	98														
θ112	20	98	20	98	20	98	20	98	20	98						
θ113	18	98														
θ114	17	99	17	99												
θ115	16	99														
θ116	15	99	15	99	15	99										
θ117	13	99														
θ118	12	99	12	99												
θ119	11	99														
θ120	10	100	10	100	10	100	10	100								
θ121	9	100														